CLAIMS

What is claimed is:

1. A method for forming a semiconductor structure, said method comprising:

providing a crystalline silicon substrate having a buffer layer thereon, wherein said buffer layer comprising at least two layers of distinct material with sharp material transitions and epitaxial alignments between the layers and between the bottom layer of said buffer layer and said crystalline silicon substrate; and

forming a group-III nitride semiconductor structure on said buffer layer.

2. The method according to claim 1, further comprising performing a surface reconstruction process to said crystalline silicon substrate.

3. The method according to claim 2, wherein said surface reconstruction process comprises a thermal annealing in ultrahigh vacuum (UHV).

4. The method according to claim 2, wherein said surface reconstruction process comprises an *in-situ* hydrogen-plasma cleaning process.

5. The method according to claim 2, wherein said surface reconstruction process comprises an *ex-situ* wet etching process.

6. The method according to claim 1, wherein said forming said buffer layer comprises:

forming a single-crystal silicon nitride layer on a silicon (111) substrate; and

forming a group-III nitride layer on said single-crystal silicon nitride layer.

7. The method according to claim 6, wherein said forming said single-crystal silicon nitride layer comprises performing a nitrogen-plasma nitridation to said silicon (111) substrate.

8. The method according to claim 6, wherein said forming said single-crystal silicon nitride layer comprises performing a thermal nitridation to said silicon (111) substrate.

9. The method according to claim 6, wherein said forming said single-crystal silicon nitride layer comprises performing a chemical vapor deposition to said silicon (111) substrate.

10. The method according to claim 6, wherein said forming said group-III nitride layer comprises:

performing an aluminum pre-deposition process to said single-crystal silicon nitride layer terminated by nitrogen surface adatoms without introducing reactive nitrogen species to form an aluminum pre-deposition atomic layer on said single silicon nitride layer;

performing a thermal annealing process to said aluminum pre-deposition atomic layer to form a single-crystal aluminum nitride

monolayer on said single-crystal silicon nitride layer; and

performing an aluminum nitride epitaxial growth process to said single-crystal aluminum nitride monolayer to form said group-III nitride layer on said single-crystal aluminum nitride monolayer.

11. The method according to claim 1, wherein said group-III nitride semiconductor structure is formed by chemical vapor deposition method.

12. The method according to claim 1, wherein said group-III nitride semiconductor structure is formed by molecular beam epitaxy method.

13. The method according to claim 1, wherein said group-III nitride semiconductor structure is a group-III nitride single layer.

14. The method according to claim 1, wherein said group-III nitride semiconductor structure is a group-III nitride multiple-layer structure.

15. The method according to claim 1, wherein said group-III nitride semiconductor structure is a gallium nitride epitaxial layer.

16. A method for growing a group-III nitride semiconductor heteroepitaxial structure, said method comprising:

providing a silicon (111) substrate;

performing a nitrogen-plasma nitridation process to said silicon (111) substrate to form a single-crystal silicon nitride layer on said

silicon (111) substrate;

performing an aluminum pre-deposition process to said single-crystal silicon nitride layer terminated by nitrogen surface adatoms without introducing reactive nitrogen species to form an aluminum pre-deposition atomic layer on said single-crystal silicon nitride layer;

performing a thermal annealing process to said aluminum pre-deposition atomic layer to form a single-crystal aluminum nitride monolayer on said single-crystal silicon nitride layer;

performing an aluminum nitride epitaxial growth process to said single-crystal aluminum nitride monolayer to form an aluminum nitride epitaxial buffer layer on said single-crystal silicon nitride layer; and

forming a group-III nitride semiconductor heteroepitaxial structure by epitaxial process on said aluminum nitride epitaxial buffer layer.

17. The method according to claim 16, further comprising performing a thermal annealing in ultrahigh vacuum to said silicon (111) substrate to form a reconstructed silicon (111) surface.

18. The method according to claim 16, further comprising performing an active hydrogen plasma cleaning process to said silicon (111) substrate to form a clean and smooth silicon (111) substrate.

19. The method according to claim 16, further comprising performing an ex-situ wet etching process to said silicon (111) substrate to form a clean and smooth silicon (111) surface.

20. The method according to claim 16, wherein said performing a nitrogen-plasma nitridation process to said silicon (111) substrate to form a said single-crystal silicon nitride layer on said silicon (111) substrate is a thermal nitridation process.

21. A semiconductor structure with a group-III nitride semiconductor heteroepitaxial structure, said semiconductor structure comprising:

a silicon (111) substrate;

a buffer layer on said silicon (111) substrate, said buffer layer having at least two layers of distinct material with sharp material transitions and epitaxial alignments between the layers and between the bottom layer of said buffer layer and said silicon (111) substrate; and

a group-III nitride semiconductor heteroepitaxial structure on said buffer layer.

22. The semiconductor structure according to claim 21, wherein said buffer layer comprises a diffusion barrier layer on said silicon (111) substrate.

23. The semiconductor structure according to claim 22, wherein the material of said diffusion barrier layer is single-crystal silicon nitride (Si_3N_4).

24. The semiconductor structure according to claim 21, wherein said buffer layer comprises an aluminum nitride layer on said diffusion barrier layer.

25. The semiconductor structure according to claim 21, wherein said buffer layer comprises a gallium nitride layer on said diffusion barrier layer.

26. The semiconductor structure according to claim 21, wherein said buffer layer comprises an indium nitride layer on said diffusion barrier layer.

27. The semiconductor structure according to claim 21, wherein said group-III nitride semiconductor heteroepitaxial structure is a group-III nitride semiconductor single epitaxial layer.

28. The semiconductor structure according to claim 21, wherein said group-III nitride semiconductor heteroepitaxial structure is a group-III nitride semiconductor multiple-layer heteroepitaxial structure.

29. A semiconductor structure with a multiple-layer buffer structure, said semiconductor structure comprising:

a silicon (111) substrate; and

a multiple-layer buffer structure on said silicon (111) substrate, said multiple-layer buffer structure having at least two layers of distinct material with sharp material transitions and epitaxial alignments between the layers and between the bottom layer of said multiple-layer buffer structure and said silicon (111) substrate.

30. The semiconductor structure according to claim 29, wherein said multiple-layer buffer structure comprises a diffusion barrier layer on said silicon (111) substrate.

31. The semiconductor structure according to claim 30, wherein the material of said diffusion barrier layer is single-crystal silicon nitride.

32. The semiconductor structure according to claim 29, wherein said multiple-layer buffer structure comprises an aluminum nitride layer on said diffusion barrier layer.

33. The semiconductor structure according to claim 29, wherein said multiple-layer buffer structure comprises a gallium nitride layer on said diffusion barrier layer.

34. The semiconductor structure according to claim 29, wherein said multiple-layer buffer structure comprises an indium nitride layer on said diffusion barrier layer.